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JCS80 U.S. PTO

UTILITY PATENT APPLICATION TRANSMITTAL <i>(Only for new nonprovisional applications under 37 CFR 1.53(b))</i>	Attorney Docket No.	S1022/8126
	First Named Inventor or Application Identifier	
	Geoff BARRETT	
	Express Mail Label No.	EM192720746US
	Date of Deposit	September 23, 1998

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APPLICATION ELEMENTS <i>See MPEP chapter 600 concerning utility patent application contents</i>	ADDRESS TO: Assistant Commissioner for Patents Box Patent Application Washington, DC 20231
<p>1. <input checked="" type="checkbox"/> Fee Transmittal Form <i>(Submit an original, and a duplicate for fee processing)</i></p> <p>2. <input checked="" type="checkbox"/> Specification [Total pages 14] 10 pages description 1 pages abstract 3 pages claims 11 claims</p> <p>3. <input checked="" type="checkbox"/> Drawing(s) (35 USC 113) [Total sheets 4] <input type="checkbox"/> Informal <input checked="" type="checkbox"/> Formal [Total drawings 1-7]</p> <p>4. <input checked="" type="checkbox"/> Oath or Declaration [Total pages 2] a. <input checked="" type="checkbox"/> Newly executed (original or copy) b. <input type="checkbox"/> Copy from a prior application (37 CFR 1.63(d)) <i>(for continuation/divisional with Box 17 completed)</i> <i>[Note Box 5 below]</i> i. <input type="checkbox"/> <u>DELETION OF INVENTOR(S)</u> Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).</p> <p>5. <input type="checkbox"/> Incorporation by Reference <i>(usable if Box 4b is checked)</i> The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.</p>	<p>6. <input type="checkbox"/> Microfiche Computer Program (Appendix)</p> <p>7. <input type="checkbox"/> Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary) a. <input type="checkbox"/> Computer Readable Copy b. <input type="checkbox"/> Paper Copy (identical to computer copy) c. <input type="checkbox"/> Statement verifying identity of above copies</p> <p>ACCOMPANYING APPLICATION PARTS</p> <p>8. <input checked="" type="checkbox"/> Assignment Papers (cover sheet & documents(s))</p> <p>9. <input type="checkbox"/> 37 CFR 3.73(b) Statement <input type="checkbox"/> Power of Attorney <i>(when there is an assignee)</i></p> <p>10. <input type="checkbox"/> English Translation of Document <i>(if applicable)</i></p> <p>11. <input type="checkbox"/> Information Disclosure Statement (IDS)/PTO-1449 <input type="checkbox"/> Copies of IDS Citations</p> <p>12. <input type="checkbox"/> Preliminary Amendment</p> <p>13. <input checked="" type="checkbox"/> Return Receipt Postcard (MPEP 503) <i>(Should be specifically itemized)</i></p> <p>14. <input type="checkbox"/> Small Entity <input type="checkbox"/> Statement filed in prior application, Status still proper and desired</p> <p>15. <input type="checkbox"/> Certified Copy of Priority Document(s) <i>(if foreign priority is claimed)</i></p>
16. Other: PURSUANT TO 35 U.S.C. §119, APPLICANT HEREBY CLAIMS PRIORITY TO UNITED KINGDOM PATENT APPLICATION NO. 9720648.6, FILED SEPTEMBER 29, 1997.	

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17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.:

☐ Cancel in this application claims before calculating the filing fee.

☐ Amend the specification by inserting before the first line the sentence:

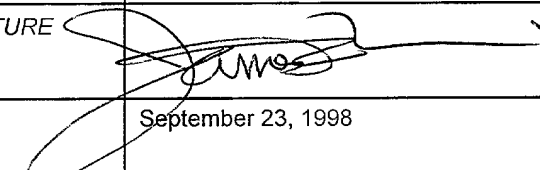
This application is a ☐ continuation ☐ divisional of application serial no. , filed , entitled , and now .

18. CORRESPONDENCE ADDRESS

Correspondence address below

ATTORNEY'S NAME	James H. Morris, Reg. No. 34,681				
NAME	Wolf, Greenfield & Sacks, P.C.				
ADDRESS	600 Atlantic Avenue				
CITY	Boston	STATE	MA	ZIP	02210
COUNTRY	USA	TELEPHONE	(617) 720-3500	FAX	(617) 720-2441

19. SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

NAME	James H. Morris, Reg. No. 34,681
SIGNATURE	
DATE	September 23, 1998

Inventor or Identifier: Geoff BARRETT

Serial No: Not yet assigned

Filed: Herewith

CHECK BOX, if applicable:

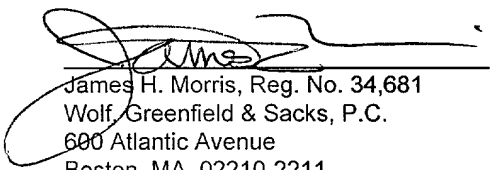
For: METHOD AND APPARATUS FOR PROVING SYSTEM
PROPERTIES☒ **DUPLICATE****Fee Calculation Sheet**

CLAIMS	FOR	NUMBER FILED	NUMBER EXTRA	RATE	FEE
	TOTAL CLAIMS (37 CFR 1.16(c))	11 - 20=	0 x	\$22	= \$ 0
	INDEPENDENT CLAIMS (37 CFR 1.16(b))	6 - 3=	3 x	\$82	= \$246.00
	MULTIPLE DEPENDENT CLAIMS (if applicable) (37 CFR 1.16(d)) +			\$	= \$ 0
				BASIC FEE (37 CFR 1.16(a))	\$790.00
	Fee for Petition for Extension of Time (if any)				\$ 0
	Total of above Calculations =				\$
	Reduction by 50% for filing by small entity (Note 37 CFR 1.9, 1.27, 1.28).				\$
	Assignment Recordation Fee (if any)				\$40.00
	Other Fees (e.g., Petition for Extension of Time), if any NOTE: Enter small-entity amount if applicable.				\$
	TOTAL =				\$820.00

1. A check in the amount of \$ 820.00 is enclosed.

General Authorization to Charge Deposit Account and General Request for Extension of Time

2. a. ☒ If the filing of any paper in this application necessitates the payment of a fee under 37 CFR §
☒ 1.16 ☒ 1.17 or ☐ 1.18, and the fee due is in an amount different from any enclosed check or if no
check is enclosed, the Commissioner is hereby authorized to charge any deficiency or credit any
overpayment to Deposit Account No. 23/2825.
- b. ☐ The applicant hereby revokes any prior authorization to charge a fee due under 37 CFR §
☐ 1.16 ☐ 1.17 or ☐ 1.18.
3. If the filing of any paper in this application necessitates an extension of time under 37 CFR §1.136(a), the
applicant hereby requests such extension of time. If the fee due is in an amount different from any
enclosed check or if no check is enclosed, the Commissioner is hereby authorized to charge any
deficiency or credit any overpayment to Deposit Account No. 23/2825.


James H. Morris, Reg. No. 34,681
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, MA 02210-2211
(617) 720-3500
Attorneys of Record
Docket No. S1022/8126
Date: September 23, 1998

Patent Application of

Geoff BARRETT
28 Devonshire Road
Westbury Park, Bristol, BS6 7NJ
GREAT BRITAIN

for

APPARATUS FOR PROVING SYSTEM PROPERTIES

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METHOD AND APPARATUS FOR PROVING SYSTEM PROPERTIES

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to a method and apparatus for reducing the complexity of a representation of a hardware system.

DESCRIPTION OF THE PRIOR ART

The first stage in synthesizing and proving the properties of a system is a compilation process in which the system is modelled by representation as a set of functions comprising:-

a first subset of functions which determines the value of system outputs as a function of system inputs, system states represented by state bits, and internal signals;

a second subset of functions which determines the values of state bits on the next clock cycle as a function of system inputs, system states represented by state bits, and internal signals; and

a third subset of functions which determines the values of internal signals as a function of system inputs, system states, and internal signals.

To enable or accelerate formal proof of the system and its properties, internal signals may be eliminated from the system model by substituting them into the functions which refer to them. In the course of this substitution, the representation of the model may become extremely large. If this occurs, it is possible to detect an explosion in the size of the representation and to suspend the substitution process while restructuring the representation to seek a reduction in size.

Typically in a compilation process, static relationships between signals in the system model can be destroyed by dynamic restructuring operations. This can lead to a further explosion later during the substitution process.

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It would be advantageous to take static relationships into account during the dynamic restructuring process.

One technique of representing functions and internal signals is by the use of binary decision diagrams (BDD's). A binary decision diagram is a representation of a digital function which contains the information necessary to implement the function. The diagram is a tree-like structure having a root and plural nodes, where the root represents the digital function and the nodes are labelled with variables. Each node has two branches, one representing the assertion that the variable labelling the node is 1, and the other representing the assertion that the variable labelling the node is 0. In a BDD, "ordering" relates to the order in which variable names are encountered during traversal of the graph. Better orderings result in fewer nodes in the graph.

SUMMARY OF THE INVENTION

According to a first aspect of the present invention, there is provided a method for selecting an order in which to sift variables in a binary decision diagram comprising:-

arranging the variables of a binary decision diagram on the nodes of a graph in which the nodes are labelled with the variables of the system such that the set of functions labelling leaves reachable from a node, correspond to the set of functions which depend on the variables labelling the node; and

traversing the graph in a depth first manner, thereby to produce a list of said labels in said selected order.

According to a second aspect of the present invention there is provided apparatus for selecting an order in which to sift variables in a binary decision diagram comprising a first store storing bits representing the variables of the binary decision diagram;

a second store; and

a processor adapted to arrange the said variables of said

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binary decision diagram in a representation of the nodes of a graph in which the nodes are labelled with the variables such that the set of functions labelling leaves reachable from a node corresponds to the set of functions which depend on the variables labelling the node; and to

traverse the graph in a depth-first manner such that said processor means outputs to said second store a list of said labels in said selected order.

According to a third aspect of the present invention there is provided a method for restructuring a binary decision diagram representative of a hardware system, comprising:-

arranging the variables of a binary decision diagram on the nodes of a graph in which the nodes are labelled with the variables of the system such that the set of functions labelling leaves reachable from a node corresponds to the set of functions which depend on the variables labelling the node; and

traversing the graph in a depth-first manner to produce a list of said labels in a selected order;

using said selected order, controlling sifting each variable.

Preferably said variables are sifted one-by-one to a deepest best location. Advantageously said variables are sifted one-by-one in said selected order to a deepest best location followed by sifting in reverse order to a shallowest best location.

According to a fourth aspect of the present invention there is provided apparatus for restructuring a binary decision diagram comprising:-

storage circuitry for storing bits representative of a set of functions as binary decision diagrams having a plurality of nodes labelled by variables;

a processor for detecting a number of nodes of said binary decision diagram, and in response to such detection, arranging the variables of said binary decision diagram on the nodes of a graph in which the nodes are labelled such that the set of

functions labelling leaves reachable from a node corresponds to the set of functions which depend on the variables labelling the node, traversing the graph in a depth-first fashion to produce a list of labels in a selected order and using said selected order, controlling sifting of variables of said binary decision diagrams;

wherein said sifted binary decision diagram is written by said processor to said storage.

According to a fifth aspect of the present invention there is provided a method for proving the properties of a hardware system comprising:-

representing said system as binary decision diagrams having a plurality of nodes labelled by variables;

substituting functions which determine variables of internal signals;

arranging the variables of a binary decision diagram on the nodes of a graph in which the nodes are labelled with the variables of the system such that the set of functions labelling leaves reachable from a node corresponds to the set of functions which depend on the variables labelling the node; and

traversing the graph in a depth-first manner to produce a list of said labels in a selected order;

using said selected order, controlling sifting each variable.

According to a sixth aspect of the present invention there is provided apparatus for proving the properties of a hardware system comprising:

storage circuitry for storing bits representative of a set of functions which represent the hardware system as binary decision diagrams having a plurality of nodes labelled by variables;

processor means for substituting functions which determine the values of internal signals into the set of functions representing said system and detecting an increase in the number of nodes of said binary decision diagram, and, in response to

Figure 5 is an optimally ordered substitution of the equations of Figures 3 and 4;

Figure 6 shows a graph of relationships between the variables of the multiplexer of Figure 2; and

Figure 7 shows an example of apparatus arranged to implement an embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A Binary Decision Diagram (hereinafter referred to as a BDD) is a directed acyclic graph representative of a Boolean function as a decision procedure based on the variables on which it depends. For instance, for the function:-

$$f = x \text{ OR } y,$$

f can be implemented by the decision procedure "if x then true else if y then true else false". Each of the "if...then...else..." constructs of this decision procedure can be represented as a node in a graph.

Referring to Figure 1, the first node 1 is labelled with the variable x and there are two branches from this first node, one 11 is "true" and the other 12 is "if y then true else false". This other branch 12 leads to a second node 2 which is labelled with the variable y, which in turn has two branches 21, 22 of which one is "true" and the other is "false".

It will be understood that although the nodes 1 and 2 are described above as being labelled with variables, nevertheless these labels could in fact refer to functions which upon evaluation would give rise to the logical values "true" or "false".

Referring now to Figure 2, a multiplexer consists of a first set of n NAND gates 10₁-10_n, each gate having two respective inputs a₁-a_n, s₁-s_n. The outputs lines b₁ and b_n of the gates are connected to an n-input NAND gate 20 having an output d.

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Thus, in terms of a system as described in the preamble to this patent application, the multiplexer of Figure 2 has system inputs (a_1-a_n, s_1-s_n) , internal signals (b_1-b_n) and a system output (d) . The output d is related to the internal signals b_1-b_n by the equation:-

$$d = \text{NOT } (b_1 \text{ AND } b_2 \text{ AND } b_3 \dots b_n)$$

and each internal signal b_i to the respective inputs a_i and s_i by the equation

$$b_i = \text{NOT } (a_i \text{ AND } s_i)$$

Thus,

$$d = (a_1 \text{ AND } s_1) \text{ OR } (a_2 \text{ AND } s_2) \text{ OR } \dots (a_n \text{ AND } s_n)$$

Referring to Figure 3 the relationship $b_i = \text{NOT } (a_i \text{ AND } s_i)$ is shown as a binary decision diagram.

Figure 4 shows the binary decision diagram representation of the expression for d in terms of the internal signals b .

By inspection, there are $3n$ variables (a_i , s_i and b_i) and there are thus $(3n)!$ apparently equally good orderings possible. However, by inspection of the overall equation for the device it would be seen that a_1 and s_1 are associated together, a_2 and s_2 are associated together and so on which means that there are in fact only $n!$ orderings which are optimal for the entire system.

An advantage of the present invention is that it enables more information about the system as a whole to be taken into account when performing operations which would otherwise not take this information into account. Failing to take the information into account can result in following paths which do not lead to a solution, or which are highly inefficient in reaching the solution.

Figure 5 shows a binary decision diagram for the multiplexer of Figure 2 in which the respective pairs of inputs are associated together.

The size of a binary decision diagram is sensitive to the order in which the variables are inspected, and efficient BDD reordering is very important. One algorithm for reordering is "sifting", wherein each variable is taken in turn and the best position of it is found by trying it in every possible position of the BDD. It is then necessary to decide which variable to take first. A known and frequently successful tool for doing this is to rank the variables according to which variable labels the greatest number of nodes and then to sift in the order of ranking.

In the present BDD, it is clear that each variable labels a single node and thus it would not be possible using known techniques to identify a highest ranking variable. Conventionally, in such a situation, an arbitrary order for sifting would be used.

The present invention makes use of a function graph which is traversed to determine an order for sifting.

As used herein, a function graph is a directed acyclic graph where the leaves are labelled with functions and the nodes are labelled with sets of variables (non-empty). The only restriction put on this graph is that a variable which is in the set labelling a node is in the "cone" of all the functions at the leaves below it and no others. This restriction plus the fact that the sets of variables must be non-empty, is enough to ensure that the graph is unique. The "cone" of a function is herein defined to be all those variables on which a function depends, either directly or through the intermediate signals on which it depends.

Using a function graph to define an ordering of the

variables in a BDD to minimise its size may be related to the register allocation technique used in software compilation in that the ordering of the variables is derived from a traversal of the function graph in such a way that no node is visited before all of its predecessors has been visited, but each node is visited as soon as all its predecessors have been visited, unless there is a race between more than one node, in which case one of the competing nodes is chosen and its subgraphs traversed first.

Figure 6 shows a function graph for the multiplexer of Figure 2 having a root labelled by b_1-b_n intermediate nodes labelled by $a_1, s_1, a_2, s_2 \dots a_n, s_n$ and leaves as shown. Traversing this function graph from the top down gives the order:-

$b_1, b_2 \dots b_n, a_1, s_1, a_2, s_2 \dots a_n, s_n$

By using this order which is derived from static information of the system, the binary decision diagrams of (in this case) Figures 1, 3 and 4 are sifted to provide an optimal order. This order is that represented by Figure 5.

It should be noted that substitution may be effected without restructuring the BDD, while monitoring the size of the BDD. If an explosion in BDD size is detected, sifting is then effected on the basis of the order provided by the present invention.

Figure 7 shows an example of apparatus arranged to implement an embodiment of the present invention. A first storage circuitry 30 stores data representative of the variables of a binary decision diagram.

The first storage circuitry has an input 32 for receiving the variables. The output 34 of the first storage circuitry is coupled to an input of a processor 40. The processor receives the variables via the output 34 of the first storage circuitry and consults a function graph by arranging the variables in a representation of the nodes of the graph such that the nodes are

labelled with the variables so that the set of functions labelling leaves reachable from a node corresponds to the set of functions which depend on the variables labelling the node, as shown in Figure 6. The processor then traverses the graph in a depth-first manner, as indicated in Figure 6 by the arrow, to construct a list of the labels in a selected order. The list is output from the processor via output 44 which is coupled the input 52 of second storage circuitry.

While the invention has been previously shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.

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What is claimed is:-

1. A method for selecting an order in which to sift variables in a binary decision diagram comprising:-

arranging the variables of a binary decision diagram on the nodes of a graph in which the nodes are labelled with the variables of the system such that the set of functions labelling leaves reachable from a node correspond to the set of functions which depend on the variables labelling the node; and

traversing the graph in a depth first manner, thereby to produce a list of said labels in said selected order.

2. Apparatus for selecting an order in which to sift variables in a binary decision diagram comprising a first store storing bits representing the variables of the binary decision diagram; a second store; and

a processor adapted to arrange the said variables of said binary decision diagram in a representation of the nodes of a graph in which the nodes are labelled with the variables such that the set of functions labelling leaves reachable from a node corresponds to the set of functions which depend on the variables labelling the node; and to traverse the graph in a depth-first manner such that said processor outputs to said second store a list of said labels in said selected order.

3. A method for restructuring a binary decision diagram representative of a hardware system, comprising:-

arranging the variables of a binary decision diagram on the nodes of a graph in which the nodes are labelled with the variables of the system such that the set of functions labelling leaves reachable from a node corresponds to the set of functions which depend on the variables labelling the node; and

traversing the graph in a depth-first manner to produce a list of said labels in a selected order;

using said selected order, controlling sifting each variable.

4. A method as claimed in claim 3 wherein said variables are sifted one-by-one to a deepest best location.

5. A method as claimed in claim 3 wherein said variables are sifted one-by-one in said selected order to a deepest best location followed by sifting in reverse order to a shallowest best location.

6. Apparatus for restructuring a binary decision diagram comprising:-

storage circuitry for storing bits representative of a set of functions as binary decision diagrams having a plurality of nodes labelled by variables;

a processor for detecting a number of nodes of said binary decision diagram, and in response to such detection, arranging the variables of said binary decision diagram on the nodes of a graph in which the nodes are labelled such that the set of functions labelling leaves reachable from a node corresponds to the set of functions which depend on the variables labelling the node, traversing the graph in a depth-first fashion to produce a list of labels in a selected order and using said selected order, controlling sifting of variables of said binary decision diagrams;

wherein said sifted binary decision diagram is written by said processor to said storage circuits.

7. A method for proving the properties of a hardware system comprising:-

representing said system as binary decision diagrams having a plurality of nodes labelled by variables;

substituting functions which determine variables of internal signals;

arranging the variables of a binary decision diagram on the nodes of a graph in which the nodes are labelled with the variables of the system such that the set of functions labelling leaves reachable from a node corresponds to the set of functions which depend on the variables labelling the node; and

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traversing the graph in a depth-first manner to produce a list of said labels in a selected order;

using said selected order, controlling sifting each variable.

8. Apparatus for proving the properties of a hardware system comprising:

storage circuitry for storing bits representative of a set of functions which represent the hardware system as binary decision diagrams having a plurality of nodes labelled by variables;

a processor for substituting functions which determine the values of internal signals into the set of functions representing said system and detecting an increase in the number of nodes of said binary decision diagram, and, in response to such detection arranging the variable of said binary decision diagram on the nodes of a graph in which the nodes are labelled with the variables of the system such that the set of functions labelling leaves reachable from a node corresponding to the set of functions which depend on the variables labelling the node, traversing the graph in a depth-first fashion to produce a list of labels in said selected order, and using said selected order controlling sifting of the variables of said binary decision diagram; and

further comprising a second store, wherein said sifting binary decision diagram is written by said processor to said second store.

9. Apparatus as claimed in claim 8 wherein said number is a threshold derived from an original number of nodes.

10. Apparatus as claimed in claim 8 wherein said number of nodes is the number of nodes which branches on a predetermined variable.

11. Apparatus claimed in claim 8 wherein said number is an absolute number.

METHOD AND APPARATUS FOR PROVING
SYSTEM PROPERTIES

ABSTRACT

A method for selecting an order in which to sift variables in a binary decision diagram by arranging the variables of a binary decision diagram on the nodes of a graph, the nodes of the graph being labelled with the variables of the system such that the set of functions labelling the leaves reachable from a node correspond to the set of functions which depend on the variables labelling the node, and traversing the graph in a depth first manner, thereby to produce a list of the labels in the selected order.

Fig. 1

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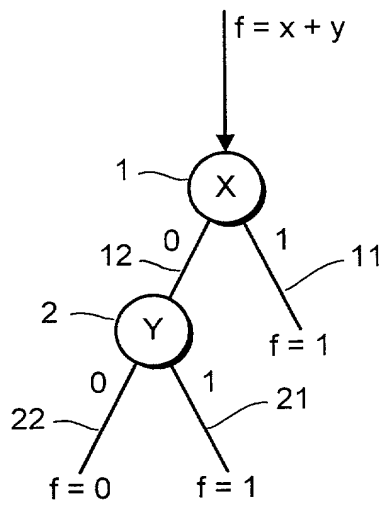


FIG. 1

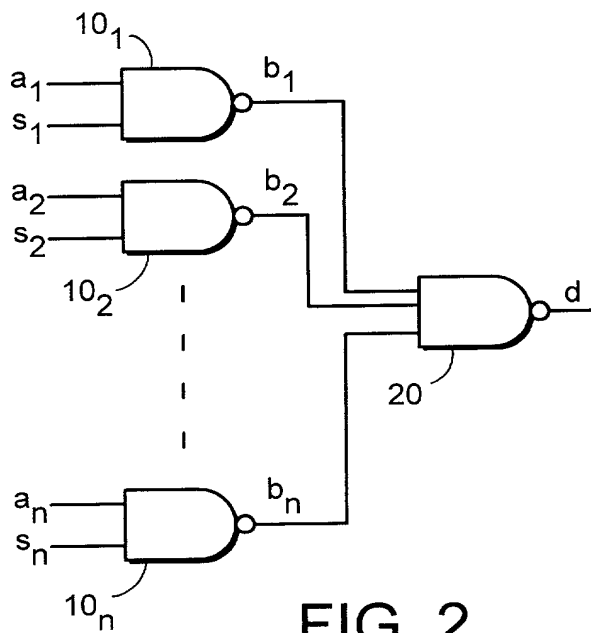


FIG. 2

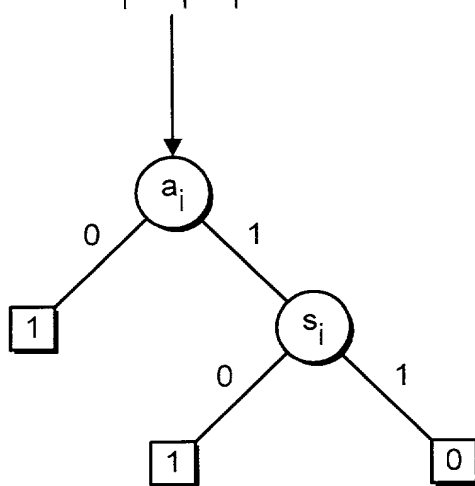


FIG. 3

$$d = \overline{b_1 \cdot b_2 \dots b_n}$$

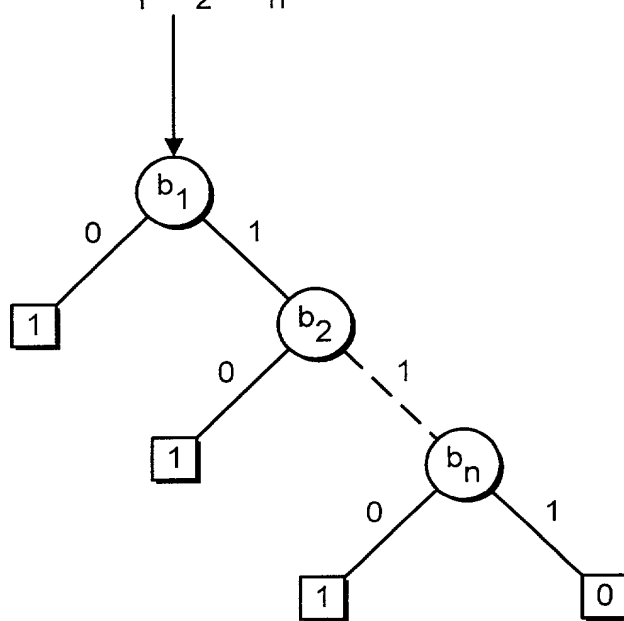


FIG. 4

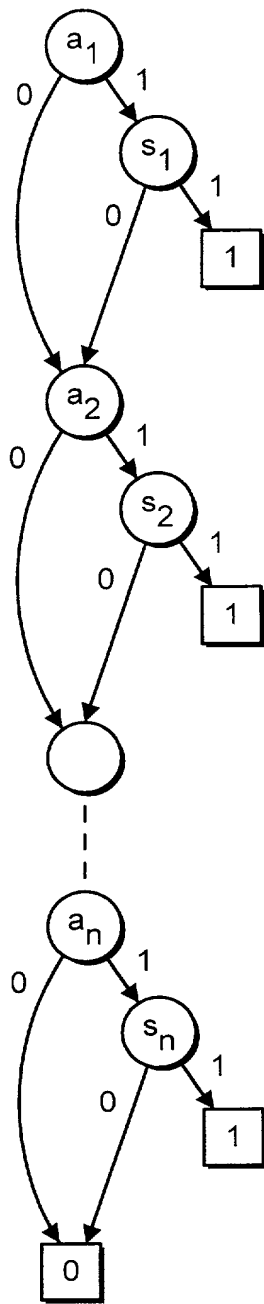


FIG. 5

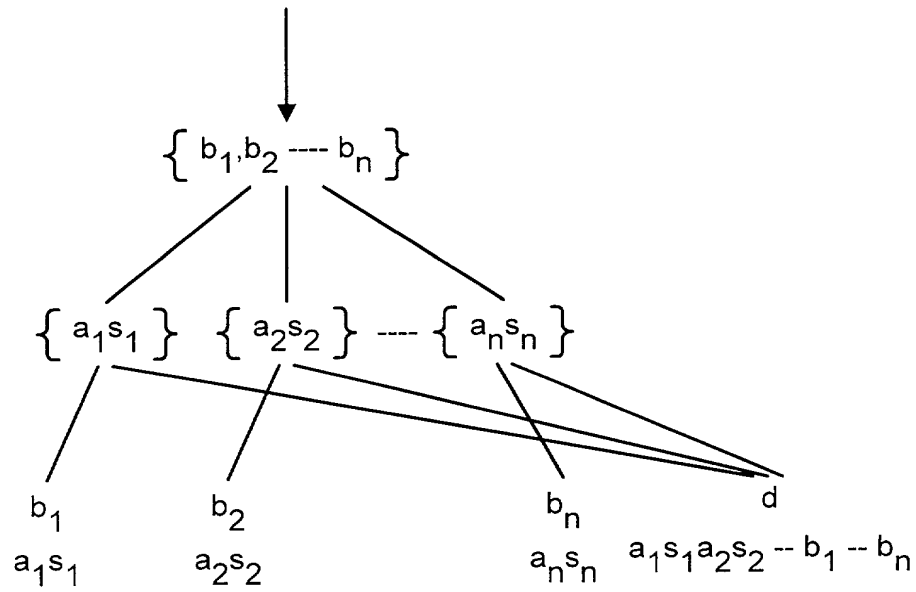


FIG. 6

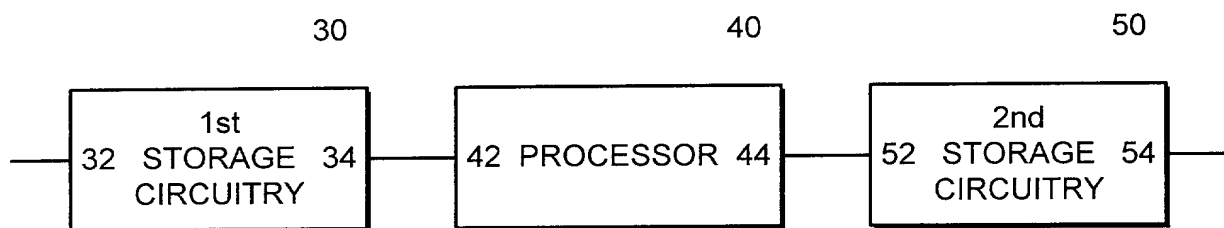


FIG. 7

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled METHOD AND

APPARATUS FOR PROVING SYSTEM PROPERTIES

the specification of which is attached hereto unless the following is checked:

[] was filed on _____, as United States Application No. _____ or PCT International Application No. _____, bearing attorney docket No. _____, and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application designating at least one country other than the United States listed below and have also identified below any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed:

Prior Foreign PCT International Application(s) and any priority claims under 35 U.S.C. Sections 119 and 365(a), (b):

9720648.6	GB	29/09/97	Priority Claimed
(Number)	(Country-if PCT, so indicate)	(DD/MM/YY Filed)	<input checked="" type="checkbox"/> YES <input type="checkbox"/> NO
_____	_____	_____	<input type="checkbox"/> YES <input type="checkbox"/> NO
(Number)	(Country)	(DD/MM/YY Filed)	<input type="checkbox"/> YES <input type="checkbox"/> NO
_____	_____	_____	<input type="checkbox"/> YES <input type="checkbox"/> NO
(Number)	(Country)	(DD/MM/YY Filed)	<input type="checkbox"/> YES <input type="checkbox"/> NO
_____	_____	_____	<input type="checkbox"/> YES <input type="checkbox"/> NO

I am the inventor of United Kingdom application number 9720648.6, filed 29/09/97, which application was filed by the assignee SGS-Thomson Microelectronics, Limited.

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below:

_____	_____
(Application Number)	(filing date)
_____	_____
(Application Number)	(filing date)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or Section 365(c) of any PCT International application(s) designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

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(Application No.)	(filing date)	(status-patented, pending, abandoned)
(Application No.)	(filing date)	(status-patented, pending, abandoned)

PCT International Applications designating the United States:

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I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

David Wolf	17,528	Anthony J. Mirabito	28,161	John N. Anastasi	37,765
George L. Greenfield	17,756	Jason M. Honeyman	31,624	Brett N. Dorny	35,860
Stanley Sacks	19,900	James H. Morris	34,681	Helen C. Kindregan	39,248
David M. Driscoll	25,075	Peter C. Lando	34,654	James M. Hanifin, Jr.	39,213
Edward F. Perlman	28,105	Gary S. Engelson	35,128	David E. Huang	39,229
Lawrence M. Green	29,384	Peter J. Gordon	35,164	Thomas M. Sullivan	39,392
Steven J. Henry	27,900	Randy J. Pritzker	35,986		
Therese A. Hendricks	30,389	Richard F. Giunta	36,149		
Edward R. Gates	31,616	Douglas R. Wolf	36,971		
William R. McClellan	29,409	Helen A. Greer	36,816		
Ronald J. Kransdorf	20,004	Elizabeth R. Plumer	36,637		
M. Lawrence Oliverio	30,915	Timothy J. Oyer	36,628		
James J. Foster	30,052	Kristofer E. Elbing	34,590		
Charles E. Pfund	17,030				
Christopher S. Schultz	37,929				
Paul D. Sorkin	39,039				
Douglas C. Doskocil	39,660				
John R. Van Amsterdam	40,212				
Barry W. Chapin	39,934				
Scott A. Ouellette	38,573				
Joseph P. Aiena	39,501				

Address all telephone calls to David M. Driscoll or James H. Morris at telephone no. (617) 720-3500.
Address all correspondence to

David M. Driscoll or James H. Morris
c/o Wolf, Greenfield & Sacks, P.C.,
Federal Reserve Plaza
600 Atlantic Avenue
Boston, MA 02210-2211

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Inventor's signature S. Panoth Date 26 May 98
Full name of sole or first inventor _____
Citizenship British
Residence 28 Devonshire Road, Westbury Park, Bristol, BS6 7NJ
Post Office Address _____

Inventor's signature _____ Date _____
Full name of second or joint inventor _____
Citizenship _____
Residence _____
Post Office Address _____